from a surface of said epitaxial layer opposite said substrate into said epitaxial layer to form respective first and a second junctions therewith; and

an isolating element positioned between said first and said second regions and extending from the surface of said epitaxial layer at least as far as said substrate for reducing an injection of current through said epitaxial layer from said first region to said second region when the first junction is directly biased, said isolating element comprising a dielectric material adjacent said epitaxial layer and polycrystalline silicon spaced apart from said epitaxial layer by said dielectric material.

13. The integrated structure according to Claim 12 wherein said isolating element at least partially surrounds said first region.

14. The integrated structure according to Claim 12 wherein said integrated structure is formed on a semiconductor chip; and wherein said isolating element has a length substantially equal to a width of the semiconductor chip and divides the semiconductor chip into two portions each respectively including said first region and said second region.

15. The integrated structure according to Claim 12 wherein the first conductivity type is P type.

16. The integrated structure according to Claim 12 wherein said first region comprises a power transistor for controlling an inductive load.

17. An integrated structure comprising:

a substrate having a first conductivity type;

an epitaxial layer on said substrate and having the first conductivity type and a conductivity less than a conductivity of said substrate;

first and second regions in said epitaxial layer each having a second conductivity type opposite the first conductivity type, said first and second regions extending from a surface of said epitaxial layer opposite said substrate into said epitaxial layer to form respective first and a second junctions therewith; and

an isolating element positioned between said first and said second regions and extending from the surface of said epitaxial layer at least as far as said substrate, said isolating element partially surrounding at least one of said first and second regions.

18. The integrated structure according to Claim 17 wherein said isolating element comprises a dielectric material.

19. The integrated structure according to Claim 18 wherein said isolating element further comprises polycrystalline silicon.

20. The integrated structure according to Claim 17 wherein the first conductivity type is P type.

21. The integrated structure according to Claim 17 wherein said first region comprises a power transistor for controlling an inductive load.

22. An integrated structure formed on a semiconductor chip and comprising:

a substrate having a first conductivity type;

an epitaxial layer on said substrate and having the first conductivity type and a conductivity less than a conductivity of said substrate;

first and second regions in said epitaxial layer each having a second conductivity type opposite the first conductivity type, said first and second regions extending from a surface of said epitaxial layer opposite said substrate into said epitaxial layer to form respective first and a second junctions therewith; and

an isolating element positioned between said first and said second regions and extending from the surface of said epitaxial layer at least as far as said substrate, said isolating element having a length substantially equal to a width of the semiconductor chip and dividing the semiconductor chip into two portions each respectively including said first and said second regions.

23. The integrated structure according to Claim 22 wherein said isolating element comprises a dielectric material.

24. The integrated structure according to Claim 23 wherein said isolating element further comprises polycrystalline silicon.

25. The integrated structure according to Claim 22 wherein the first conductivity type is P type.

26. The integrated structure according to Claim 22 wherein said first region comprises a power transistor for controlling an inductive load.

27. A method for making an integrated structure comprising:

providing a substrate having a first conductivity type;

growing an epitaxial layer on the substrate having the first conductivity type and a conductivity less than a conductivity of the substrate;

forming first and a second regions in the epitaxial layer having a second conductivity type opposite the first conductivity type, the first and second regions extending from a surface of the epitaxial layer opposite the substrate into the epitaxial layer to form respective first and a second junctions therewith; and

forming an isolating element for reducing an injection of current through the epitaxial layer from the first to the second region when the first junction is directly biased by

forming a trench between the first and second regions extending from the surface of the epitaxial layer at least as far as the substrate,

forming a dielectric material layer in the trench, and

forming polycrystalline silicon on the dielectric material layer to fill the trench.